FAULTRACK©

UNIVERSAL
FAULT ISOLATION PROCEDURE
FOR DIGITAL LOGIC

FLUKE TRENDAR
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INTRODUCTION

Today's electronic sub-assemblies are universally designed using soldered components on printed circuit boards. Tens of millions of these board assemblies must be production tested before completed products can be tested and shipped. The value of a finished printed circuit board may range from $50 to $500 or more. Thus, defective boards are not throw-aways. Factory test technicians by the thousand are employed to troubleshoot and repair them. Large investments in semi-automatic testers are readily justified. When these boards fail in the field they are rarely scrapped. Rather, they are laboriously diagnosed and repaired by field service personnel on the spot or sent to service centers for repair. (One U. S. electronic manufacturer told TRENDAR that they maintain a widespread spare board inventory worth $50 million because of their limited ability to troubleshoot and repair boards in the field.) Most production test and field service troubleshooting is performed *manually* by technicians who depend on their personal knowledge and immediate experience with the circuit boards in question. They generally use lab instruments, meters, counters and oscilloscopes. The majority attempt to interpret scope waveforms to lead them to defective performance. Thus, troubleshooting of circuits has developed as a rather "cut and try" art. The board-repair productivity of personnel and attendant high costs have been primarily dependent on the caliber of the technician. The excuse has been that each circuit board has its own properties and specifications, and a more scientific approach has not been practical.

Troubleshooting of defective *digital* logic circuits has also been treated as an art. A technician has traditionally probed around with his scope, seeking abnormal activity of waveforms. Logic circuits differ from analog circuits. They follow specific Boolean ("truth-table") relationships. A given array and sequence of input patterns ('1's and '0's) will cause a repeatable set of internal IC state responses and circuit output responses. This is the basis of all functional logic testing. Fluke TRENDAR has demonstrated that functional go-no-go testing with high confidence results from comparing functional responses to those of a known-good board. It follows that fault diagnosis need not be left as an art.

Rather, it is practical to extend the functional comparison of a board (or an individual IC) to a more scientific troubleshooting method, using comparative tools specifically designed to do this.

Fluke TRENDAR is the first to create these practical tools and to delineate the scientific method, FAULTRACK, a universal troubleshooting procedure for digital logic. What makes this possible? Simply, any logic configuration, even an individual IC, will produce the identical functional responses as a like configuration when both experience the same excitation sequences. A fault in a logic circuit will leave a "track" . . . a path from the fault to a board output where circuit activity has caused digital responses that differ from normal. This track of abnormal responses can be found and backtracked to its cause. All troubleshooting is comparative in nature. With FAULTRACK three alternative equipment approaches can be used to find the defective node.

Simple five-step universally applicable procedures are described. These five-step methods are summarized in Figures 1, 2 and 3 according to which tools are used. Any technician can be quickly trained to rapidly troubleshoot today's digital logic boards with FAULTRACK.

FAULTRACK 2000

1. Compare IC's at failed board output.
2. Backtrack IC input failures on previous IC's.
3. Locate a previous IC stage with only output failures.
4. Perform Node Analysis to determine fault cause.
5. Repair board or replace part.

Figure 1

FAULTRACK 1000

1. Check node transition counts at board outputs.
2. Backtrack bad counts on IC inputs.
3. Locate a previous IC stage with only output count failures.
4. Perform Node Analysis to determine fault cause.
5. Repair board or replace part.

Figure 2

FAULTRACK 200

1. Check input IC's for toggling activity and failures.
2. Check subsequent IC's and backtrack any stuck pins to origin.
3. Test IC's systematically toward board output.
4. Perform Node Analysis on failed nodes to determine fault cause.
5. Repair board or replace part.

Figure 3

Analog vs Digital

In troubleshooting analog sub-assemblies, the most common tools in use are a VOM or a digital multimeter and an oscilloscope. Measured voltages and waveforms are *compared* to correct values at successive circuit stages until an abnormal comparison of input signal to output signal is found. For example, if a technician examining the circuit stage in Figure 4 sees the 'scope waveforms shown in Figure 5, he knows he has located the faulty circuit stage because he has lost his analog waveform. If node voltages and component checks are OK, the amplifier itself can be assumed to be bad. Although the example is a simple one, the method and tools (supplemented perhaps by a counter) are sufficient for the majority of analog troubleshooting. Digital logic troubleshooting is seldom as straightforward. Consider, for example, the circuit stage shown in Figure 6. Even if the waveforms

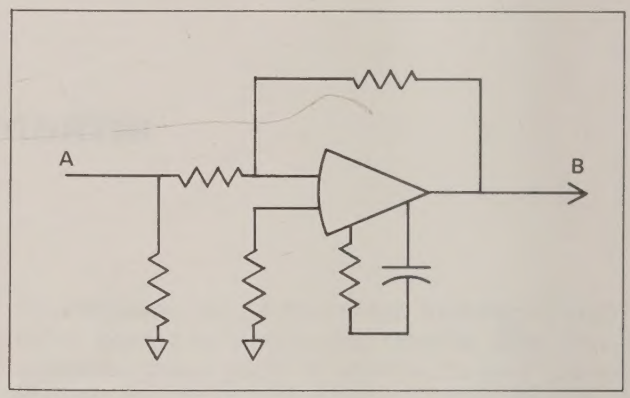

Figure 4. ANALOG CIRCUIT EXAMPLE

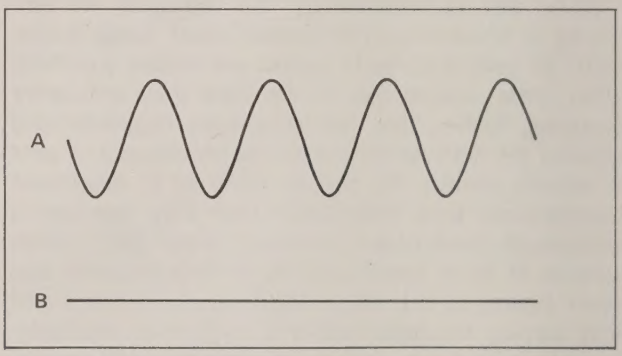

Figure 5. ANALOG WAVEFORMS

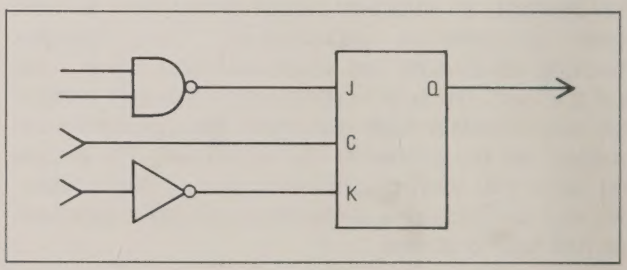

Figure 6. DIGITAL CIRCUIT EXAMPLE

can be examined as in Figure 7, (no mean feat with a dual-channel oscilloscope) it is not immediately obvious that the flip-flop is defective. (At t_4 the Q output should change from a high to a low. It doesn't, indicating a functional IC fault.)

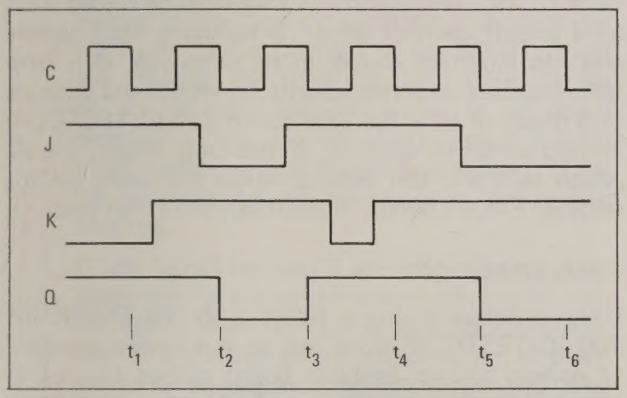

Figure 7. DIGITAL WAVEFORMS

Yet this is also a simple digital example. Obviously, analog and digital troubleshooting present different problems.

Troubleshooting Basics

All troubleshooting (and in fact, all testing) has at its base a ***comparison***, comparing what is there to what should be there. In analog circuits the comparison tends to be clear. The problem often involves making sufficiently precise measurements to allow a valid comparison. In digital circuits, voltage precision is seldom required. In this case, the difficulty involves seeing what is there, a task which is not at all simple with a VOM and scope, and knowing what should be there. The latter is made especially difficult by the number of logic elements in even a single logic family such as TTL and the fact that the "correct" output for a logic element may depend not only on the present logic states but also the past history of up to ten input signals! Clearly, what is needed to speed fault isolation in digital circuits is a combination of tools and methods which will solve the twin problems of seeing what is going on and knowing what should be going on.

The Fluke TRENDAR family of Digital Test Instruments

In both analog and digital sub-assemblies, the orderly flow of data from inputs to outputs should make possible generalized troubleshooting procedures. This has not occurred for digital circuits due to the lack of a proper set of troubleshooting tools. Because of this, Fluke TRENDAR has designed the family of digital test instruments described in Appendix 1. Spanning applications from high volume production test to field service, these instruments share the use of high test rate functional comparison techniques. Direct functional comparison has growing acceptance as the preferred method of digital troubleshooting. It eliminates the need for a technician to attempt to observe and analyze complex digital bit streams. Instead, ***the test instrument*** examines the digital data, compares it in real time with correct circuit behavior and presents only failure indications to the technician.

The power of the TRENDAR approach to troubleshooting lies in the fact that known-good reference circuits automatically provide the data against which circuit behavior is compared. In the TRENDAR 2000, the operation of a digital PC board being tested is compared directly to the behavior of a reference board being exercised by the same input signals. In addition, IC's on the unit under test can be compared to reference IC's which are receiving inputs derived directly from the unit under test.

With the TRENDAR 1000 LOGICTESTER, the need for an operating reference circuit board in field service locations is eliminated by using normal transition count totals as an immediate reference. The total number of logic state transitions which occur at a suspect circuit node during a fixed length test are the basis for troubleshooting.

With the TRENDAR 200 IC TESTCLIP the functional behavior of an IC operating on a board under test is compared to a reference IC which received the same input signals seen by the IC under test.

FAULTRACK – A UNIVERSAL LOGIC TROUBLESHOOTING METHOD

The advent of the Fluke TRENDAR line of digital test instruments made possible a generalized troubleshooting procedure for digital circuits called FAULTRACK. Logic malfunctions will leave a "track" of abnormal logic states in the operating logic. These improper states can be detected and backtracked to their cause. In order for this procedure to be valid, only two conditions must be met: 1) The logic board must be operating (either on an extender card or in an exerciser/tester such as the TRENDAR 1000 or 2000) and, 2) All sequential logic must be initialized by circuit operation or of such a nature that initialization can be forced. When these conditions are met, FAULTRACK can be used as described in the following sections. Since the

details of the procedure vary depending on which TRENDAR tester is being used, the description is divided into sections for each tester.

FAULTRACK 2000

The TRENDAR 2000 operates two boards in parallel, a known-good reference board and a unit under test (UUT). Both see the identical test pattern sequence. If both are good, there should be no failure indication. If there is a fault on the UUT, direct board-to-board comparison indicates to the operator the pin number of the first board output failure during the test sequence. This failure usually represents the end of the shortest circuit "track" of abnormal states from the fault node to the board edge. Thus tracking in reverse on this path provides the fastest route to the faulty node. Using the IC monitor clips to compare IC pin activity on the UUT to corresponding IC activity on the reference board, the track can be followed back to the faulty circuit node.

(Individual pin probes are provided where tightly assembled components prevent the use of the IC clips). The procedure with all its specific conditions is covered in Appendix 2. Its five key steps are summarized in the box of Figure 1.

Fault backtracking is based on the board-to-board comparative behavior of IC inputs. If the inputs do not compare, this tells the operator that that IC received input data (states) different from the "standard" signals received by the corresponding IC on the reference board. Thus, the fault lies upstream and is causing improper signals to migrate down the signal path to the IC in question. The operator moves his comparison clips upstream to the source IC and repeats his comparison. Output(s) would be expected to fail, but he seeks input results as his primary criteria. When an IC is reached with only output failures, the faulty node has been identified. When a fault circulates through a loop of logic, all IC's in the loop can show both input and output failures. In this case, in-circuit IC testing with the TRENDAR 2000 will effectively "break" the loop, since only the faulty node will show as a failure. FAULTRACK Node Analysis as described below provides a rigorous procedure for identifying the specific cause of the fault, eliminating the majority of "cut and try" IC replacements and sliced paths.

FAULTRACK 1000

With the TRENDAR 1000 LOGICTESTER, direct comparison is replaced by indirect comparison, using transition count totals as an intermediate reference. The backtracking technique, however, is identical to that used on the TRENDAR 2000. Its five key steps are summarized in Figure 2. Outputs are surveyed with the transition counting probe to locate output failures. Once a failed output has been found, the track of incorrect transition totals can be traced back to a circuit element which is receiving valid signals and has incorrect counts at its output(s). If a loop failure causes incorrect counts on inputs and outputs of a group of IC's, the TRENDAR 200 IC TESTCLIP is used to check each IC in the loop. Again, the IC which fails this test tells us where the faulty circuit node is. FAULTRACK Node Analysis is then used.

FAULTRACK 200

When a circuit board is tested with the TRENDAR 200 IC TESTCLIP alone, we do not have a standard of comparison to establish board output failures. If the board is operating and can be initialized, FAULTRACK can still be applied at the IC level. Since there may be no reason to suspect any particular IC more than another, we can simply start with the input IC's or the lowest number IC (7400, for example) and test all IC's of this type. The five key steps are summarized in Figure 3. A valid test requires that active inputs toggle and sequential logic is initialized. If a stuck input is detected, it can be backtracked as in the FAULTRACK 2000 and 1000 procedures. The operator proceeds to testing subsequent IC's until an IC with only output failures is located. At this point, FAULTRACK Node Analysis is again used and the fault is repaired.

FAULTRACK Node Analysis

Once failures have been found at the output of an IC, it is necessary to determine the actual fault which is causing the failures. In a field service application, it may be reasonable to assume the cause of failures is a defective IC, but in the general case board faults can also be involved. Even where a board fault is not the cause, the operator must find out which of the IC's connected to the faulty node is defective. Using the Logic Monitor on the TESTCLIP or the Logic States Display on the TRENDAR 2000, the fact that active inputs on the failing IC are toggling is verified. This is mandatory with sequential logic elements to ensure that initialization can occur. If there are inputs which are not toggling, the signal flow is probably being interrupted upstream. The TESTCLIP or IC clips are moved to the preceding IC(s) until inputs do toggle and one or more outputs fail. Using the failures indication and the Logic Monitor of the TESTCLIP (or the Failures and Logic States Displays on the

TRENDAR 2000), node analysis becomes a simple two step process:

1. The first step is to determine whether failing output(s) are toggling using the Logic Monitor (or Logic States Display). If the failed outputs are toggling, the fault may be a solder bridge to an adjacent pin or trace. If no board problem exists, the IC being tested is most likely defective and should be replaced. If the failing output(s) are not toggling, proceed to step two.
2. If the failed output(s) are stuck high or low, there may be a short circuit on the board from the faulty node to V_{CC} or ground. Otherwise the fault is either at the output of the IC being tested or at the input of a following IC. The cause can be located by use of the specific procedure of Appendix 5. Old fashioned methods usually rely on trial changeouts. However, a stuck high failure comes more often from a driving IC (output) and a stuck low failure is more often caused by a receiving IC (input). Use of the systematic procedure of Node Analysis described in the Appendix will minimize false IC changeouts and lost inventory caused by board damage.

CONCLUSION

Logic troubleshooting requires both the proper tools and a procedure which applies to all circuits. The combination of TRENDAR's digital testing products with FAULTRACK provide for the first time a generalized process which can be used across the broad range of digital troubleshooting requirements. The benefits that result include faster logic fault isolation and the virtual elimination of cut-and-try troubleshooting. Not only are direct costs reduced in both factory and field, but both doubtful boards that never leave inventory and scrap caused by troubleshooting damage can be prevented.

APPENDIX 1 —

EQUIPMENT

FLUKE TRENDAR 2000 GENERAL PURPOSE TEST STATION

The TRENDAR 2000 is a high speed functional test station for go-no-go testing and fault isolation of digital logic. A comparative tester, it operates a known-good board and a unit under test (UUT) in parallel at rates up to 4 million tests per second on all pins. The boards are operated by signals assigned from the built-in 128 pattern generators. These generators provide dual-buffered bit streams of five classes, three special pseudo-random codes, Gray Code and eight-phase pulse streams. Optional programmable generators allow creation of specially tailored test sequences.

No software is required. "Programming" is the procedure of assigning pattern generators with appropriate excitation statistics to the various inputs to create total internal node activity. Fault coverage is verified by faulting UUT nodes and checking speed of failure detection. Universal interconnect fixtures hold the "program" in the form of a wire jumper matrix and interface the boards to the test station. The TRENDAR 2000 is unexcelled in diagnostic ability. Troubleshooting faulty boards is a straight-forward technique which moves step-by-step from failure detection to fault isolation. It is based upon the fact that the Test Station applies identical and repeatable input patterns to the Unit Under Test (UUT) and the Reference Board operating alongside it. If outputs fail to compare between the two, it is clear that a fault exists somewhere between UUT inputs and outputs. The fault can be located by an unskilled operator simply by following the circuit path along which the failure propagated to the board edge. The operator starts with a failed output and traces back to the node where the failure originated.

The operator is assisted in the fault isolation process by ten different diagnostic aids built into the TRENDAR 2000. These are:

- Board edge Comparison of Inputs and Outputs
- Logic States Display of UUT Inputs and Outputs
- Board-to-Board Comparison of 14 and 16 pin DIP IC's
- Logic States Display of UUT at 14 and 16 pin DIP IC's
- Board-to-Board Comparison of Single Circuit Nodes
- Counter Display of Failed Test Count
- In-Circuit IC Test for 14 and 16 pin DIP IC's
- Manual Override Controls for all Inputs
- Continuously Variable Test Speed for differential propagation delay measurements
- Automatic V_{CC} Margin Checks with Manual Override

These tools enable a modestly trained operator to pinpoint not only simple stuck pin faults, but multiple faults, loop faults and faults that prevent initialization of sequential logic. Economic analysis will demonstrate a three to five times superiority in cost effectiveness over alternative equipment. See bulletins 110, 111, 113 and 160 for added data.

FLUKE TRENDAR 1000 LOGICTESTER

The TRENDAR 1000 is a portable suitcase size tester fully program compatible with the TRENDAR 2000. It is utilized as follows:

1. As an additional diagnostic station where the test capacity of a single TRENDAR 2000 is reached.
2. As a stand alone go-no-go and diagnostic unit for low board-volume production applications.
3. As a field service tester for use on-site or in regional service centers.

The LOGICTESTER applies identical test sequences at the same multi-megahertz test rates as does the TRENDAR 2000. The same 128 pattern generators are incorporated. It does not use a reference board, but tests by counting transitions on circuit outputs. These counts are compared to previously established normal counts and are the basis for go-no-go testing and troubleshooting. It can measure positive and negative pulse widths and perform a marginal V_{CC} check as well. The TRENDAR 200 IC TESTCLIP is supplied as an integral part of the LOGICTESTER for added troubleshooting capability. See Bulletins 120, 121, and 123 for added data.

FLUKE TRENDAR 200 IC TESTCLIP

The TESTCLIP is a superior combination of three separate logic diagnostic tools: a logic probe, logic states clip (showing state behavior of 14 or 16 pin IC's) and an in-circuit IC tester. Fashioned from low drain high impedance circuitry, the tester does not adversely load active pins. It compares the behavior of a board IC to that of a reference IC plugged into the case. Functional behavior to Megahertz rates is checked. Single or multiple instantaneous node faults are flashed to the operator on the integral display. Single or total pin behavior can be observed. The behavior of a nearby critical node can also be observed with a small extender probe.

The reference IC is mounted on a conventional long-pin IC socket. "Programming" is accomplished by substituting half-length pins at IC outputs. The TESTCLIP will automatically check IC's at V_{CC} levels from .5V to 10V. A board on an extender or being operated by a tester can be completely verified using the TESTCLIP alone. Board faults as well as IC faults can be effectively isolated. See Bulletins 130 and 131 for added data.

APPENDIX 2

FAULTRACK 2000 - DETAILED DESCRIPTION

FAULTRACK 2000 is one version of a *universal* procedure for systematically troubleshooting digital logic. This version incorporates the use of the TRENDAR 2000 General Purpose Test Station. Two identical logic circuit boards are operated in parallel, a reference and a unit under test. They undergo the same input signal patterns. The identical pattern sequence repeats for each test. The specific sequence depends upon which generators were assigned during programming. Non-correspondence in functional behavior of the two boards is detected as a failure. FAULTRACK 2000 is a systematic procedure of

backtracking the non-correspondence to the causal defect or fault. In thumbnail version, FAULTRACK 2000 is summed up in Figure 1. A detailed flow diagram is summarized in Figure 8. Let us follow the procedure through and add a few comments.

STOP-ON-FAIL mode is set at (1). It catches the first failure after an initialization sequence which is automatically applied in the AUTO TEST mode. If the board passes, it is good and the next board is tested. A board failure will halt the test station on a specific test count, and the failed output number(s) will be displayed, as indicated at (2). Repeating the test again will usually cause the failure to appear at the same test step, telling the operator that the failure is most likely catastrophic. Marginal or intermittent failures cause the test count at failure to vary. If the first failure occurs on count zero (after initialization), then the FAULTRACK procedure is carried out using the CONTINUOUS RUN mode.

At (3) when multiple failure indications occur at first failure, any of them can be chosen as a beginning point. The speed of troubleshooting should not vary significantly, as failure indications which arrive at the circuit outputs simultaneously have probably traversed a similar number of stages. At (4) we begin our reverse tracking into the circuit, following the circuit path which propagated the non-correspondence to the circuit board output. We clip buffered IC clips onto the IC's which drove the failed output pin (on the UUT) and repeat the test. A "pass" indicates lack of continuity between this final IC and the board output. Typically, we expect a failure indication which takes us to (5). An output pin failure indication (lack of comparison between corresponding output pins on the reference and UUT IC's) tells the operator that input signals corresponded (both IC's received identical pattern sequences) but the output node does not track.

At this point we branch to Node Analysis explained in Appendix 5.

If an input pin failed, it tells the operator that the fault is further up the signal stream and the IC received non-corresponding inputs. At this point the test count at failure may be the same as the previous failure count or lower, depending upon truth-table coincidence for combinatorial logic or clocking action of sequential logic.

Step (6) covers the general case where the operator may have back-tracked to the board input edge. An input failure at the board edge can come only from inputs shorted together or an open circuit (which would be displayed as a stuck input pin in the Logic

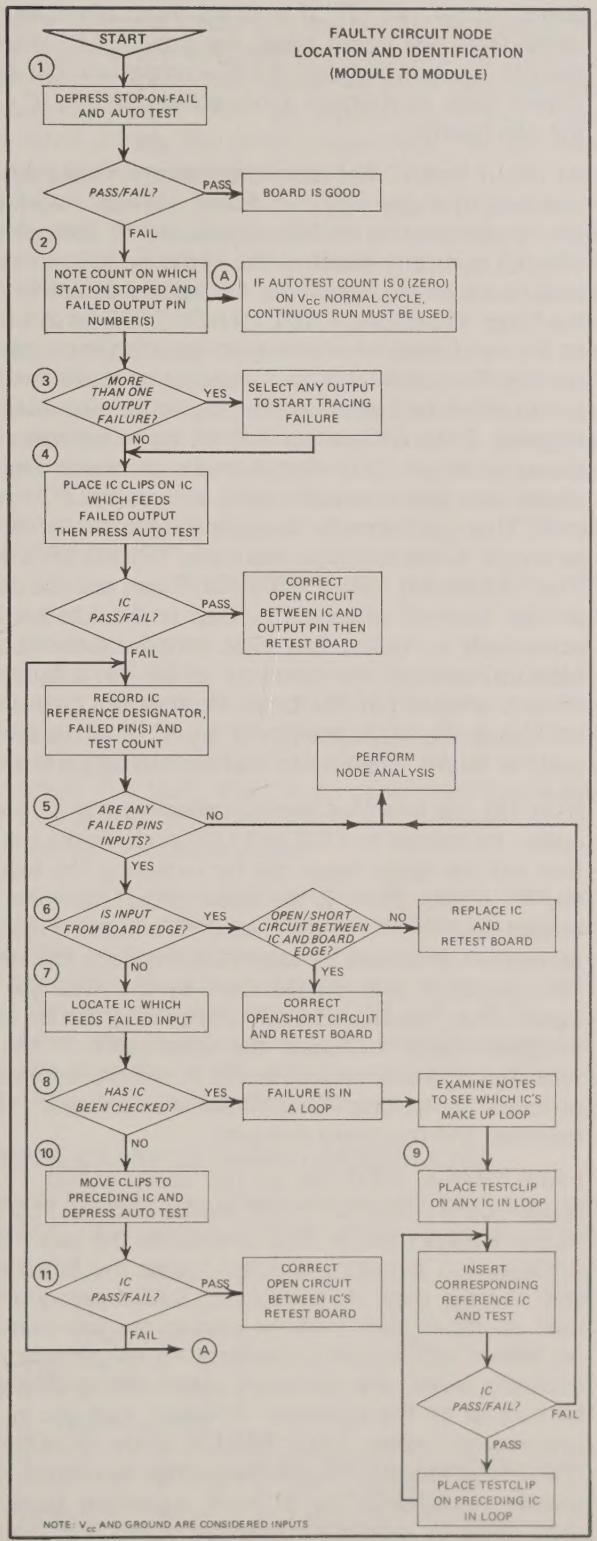

Figure 8. FAULTY CIRCUIT NODE LOCATION AND IDENTIFICATION (MODULE TO MODULE)

States mode). At (7), if a failed input pin does not come from the board edge, the previous IC driving the pin is identified and the IC comparison clips are moved back to monitor those corresponding IC's on the two boards.

At (8), if that IC has been checked previously during this test, the operator has found himself tracking a loop (feedback) fault. Board-to-Board IC comparison will not generally identify the faulty node in a closed loop, because input failures will appear at each IC in the loop. Therefore, FAULTRACK 2000 takes a step to the next level of tracking comparison, in-circuit IC testing. To use in-circuit IC testing to its fullest the circuit must be operating. That is, active pins must be toggling. Then comparison can be made between the behavior of an IC in circuit and a corresponding IC which sees the identical inputs as does the IC in circuit. This has formerly been accomplished with the in-circuit IC test option with the TRENDAR 2000. The TRENDAR 200 IC TESTCLIP can also be used. At (9), each IC around the loop is checked until a node fault is found. The logic states display (Logic Monitor) enables the operator to see pin activity. If there is a stuck pin, the Logic Monitor can be used to backtrack the stuck activity IC-by-IC until the source node is found. Then node analysis can be performed.

If at (8) the operator had not checked the IC previously, he moves to (10) and (11) and checks the IC that fed the failed input pin by repeating the test. If the IC passes there is an open circuit between its output and the formerly tested IC's input. This can be verified of course by observing the stuck (floating) pin condition that would exist at the step (5) IC input. The TRENDAR 2000 pin probes can be used as signal tracers to locate the open point. If the IC fails, the operator returns to (5) in the procedure and proceeds as before. After faults are repaired, (1) is repeated and the board will pass.

FAULTRACK 2000 can be run using AUTO TEST and/or CONTINUOUS RUN modes. AUTO TEST is nearly always used at first to provide the automatic initialization sequence and to provide the failed test step number data. As the FAULTRACK procedure is used to move back into the circuit, the test number on failure will typically decrease. In the presence of multiple faults, the minimum count failure data can be helpful to the operator. However, it is also quite practical to utilize FAULTRACK in the CONTINUOUS RUN mode. One quite effective technique that speeds troubleshooting in some situations (such as loop faults or multiple interactive faults) is to use the pattern generator override switches. All assigned generators are turned off, then enabled one at a time until an output failure is detected. This first-appearing failure is isolated using the normal FAULTRACK procedure. Then additional pattern generators are enabled until other failures are found or the board passes. Thus, the circuit has been conveniently partitioned and troubleshooting simplified.

The TRENDAR 2000's pattern sequence continually changes in CONTINUOUS RUN. A severe test to build a very high confidence level is to run 100 million or so continually changing pseudo-random patterns. The board can be further challenged by lowering V_{CC} with the V_{CC} LOW switch.

FAULTRACK 2000 – SIMPLE BOARD-TO-BOARD TROUBLESHOOTING EXAMPLE

Consider as a first example the circuit illustrated in Figure 9, with the ground fault (solder bridge) shown on pin 5 of IC-10. We will assume that the fault propagates to the board edge as a failure in AUTO-TEST on pin 9 on test count 34,190-N. (Since the

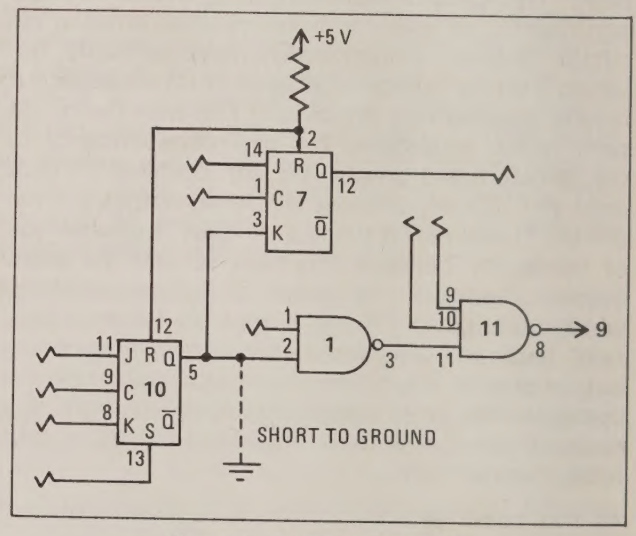

Figure 9. BOARD-TO-BOARD

test counter resets at the end of each cycle of an AUTO TEST, we add the letter -N, -H, or -L to signify the V_{CC} Normal, V_{CC} Hi, or V_{CC} Lo portions of the test). The operator will begin troubleshooting by placing the IC clips on IC-11 and depressing AUTO TEST. The IC Display will indicate failures on pins 8 and 11 at 34,190-N. Since pin 11 is an input, he moves the clips to IC-1 and tests again. This time he finds a failure on pin 2 at count 18,693-N. (Pin 3 does not fail because, for the sake of illustration, we are assuming that pin 1 does not go Hi until 34,190-N). Since pin 2 is an input, the operator pro-

ceeds to check IC-10 where he finds that pin 5 fails on count 18,693-N. Since no input failures have occurred, we have isolated IC-10-5 as the faulty node. It is now necessary to determine the actual fault which could be either a bad IC-10, IC-1 or IC-7 (Fan-out IC's) or a defect on the traces connecting the three. In our example of a solder short to ground, this would be located by an ohmmeter check and visual inspection. If the fault were a bad IC, it could be located by FAULTRACK Node Analysis.

FAULTRACK 2000 — FAILURES ON TEST COUNT 0 (ZERO)

The example presented above represents a case in which the two boards ran through some portion of the test before failing to compare. When a board fails at or near count 0-N (zero with V_{CC} Normal) special techniques may be necessary. During an AUTO TEST of length n, the first n patterns are fed to the two boards with no comparisons being made between the two boards. This initialization cycle is provided to exercise the two boards enough to get them into identical logic states without any false "failures" caused by the arbitrary states which the boards may have taken when power was first applied. There is no testing (comparisons) going on before count 0-N. Therefore, if the output(s) of a ***sequential*** logic element show a failure at count 0-N, it does not necessarily mean that the fault node has been found. A prior input failure may have occurred during the initialization sequence. The fault isolation procedure is illustrated by the following example which is based upon the circuit shown in Figure 10.

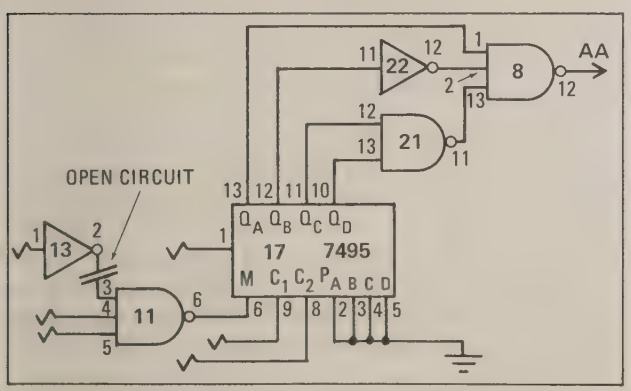

Figure 10. FAILURE AT COUNT ZERO

Let us begin by assuming a failure on count 1092-N at output pin AA. By board-to-board IC comparison, the operator locates a failure on IC 8-13 at count 532-N. This in turn leads him to a failure on IC 21-12 at count 0-N. Checking IC 17 board-to-board, we have a failure at count 0-N on pin 11, an output. At any count ***above 0-N***, we would say that IC 17-11 is the faulty node! But, since we have detected the failure ***at count 0-N***, an input failure may have occurred during the initialization cycle. We can find out by performing an In-Circuit IC Test of IC-17. The operator inserts a reference 7495 and in this example finds that the IC passes. (Board output AA will still fail at count 1092-N). This means that IC-17 itself is good and the failure at IC-17 was caused by an input failure. We can't detect the input failure which occurred during initialization, so we need to catch it the next time it occurs, in a way in which the test station won't stop on the failures already found. We can do this by testing in the FAIL INHIBIT mode, using the Logic Probes. In this mode, only a failure detected by the IC Clips or the Logic Probes will stop the test. This allows the operator to detect the input failure the first time it re-occurs ***after*** the end of initialization. In our example, if he places the probes on IC 17-1 and runs an AUTO TEST, the test will proceed to the end with no failure detected by the probes. Moving to IC 17-6, the probes will detect a Failure and stop the test at count 3673-N. This leads the operator to IC 11, where the IC Clips show a failure on pin 3 on count 3219-N. Testing IC-13, no failure is detected. The fault, then, is an open circuit between IC 13-2 and IC 11-3, easily located via visual inspection and an ohmmeter check.

In summary, troubleshooting with FAULTRACK 2000 always involves working from a failed output to the fault node. Test results are based upon comparisons made by the test station between either the UUT and Reference Boards or a UUT IC and a Reference IC. Thus, the operator is not required to understand exactly how the circuit actually works, but he need only follow the logical steps of the procedure.

SIMPLE EXAMPLE USING LOGIC STATES

Figure 11 shows a circuit which will illustrate the location of a common fault mode found in 7493

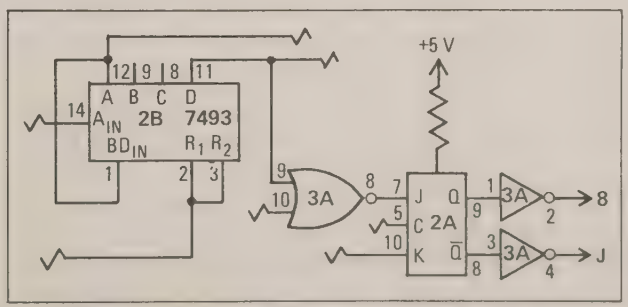

Figure 11. EXAMPLE USING LOGIC STATES

counters. In this case we're assuming the fault first appears as a failure at outputs 8 and J. It should be noted that when two or more outputs fail on the same count, there is no difficulty. If there is only one fault, any failure will lead the operator to it. If there are multiple faults they must be located one at a time and it doesn't matter which is located first. Testing with the IC Clips on IC 3A shows failures at pins 1,2,3, and 4. Checking IC 2A we find an input failure on pin 7. This leads us to 3A where we see failures on pins 8 and 9. Pin 9 comes from 2B and here we find failures at pins 8 and 11. Since there are no input failures, we've located the fault nodes. With the two bad nodes (one of which is unused) we can rule out a faulty IC on the fan-out(s) from the fault node. Furthermore, since the two bad pins aren't adjacent, a solder short is less likely. Thus, before further testing, we should examine the logic states at each of the pins on IC 2B. The operator does this by making sure the FAILURES/LOGIC STATES switch is in FAILURES, depressing CONT RUN two times and then switching to LOGIC STATES. The IC Display now indicates light-on for +5V and light-off for ground. Viewing the display, the operator sees +5V at pins 2,3,8,10,11, and 14 and ground at all other pins. Now, on a 7493 +5V on 2 and 3 is a Reset and pins 8,9,11 and 12 should all go low. Armed with this knowledge, the operator knows that he either has a short to V_{CC} on 2B-8 and 2B-11 or 2B is bad. Node Analysis is performed to determine the cause.

APPENDIX 3 —

FAULTRACK 1000 - DETAILED DESCRIPTION

The Fluke TRENDAR 1000 LOGICTESTER applies a selected test pattern sequence at rates up to 4 million tests per second. Proper logic board operation is determined by probing circuit output transitions, and comparing transition counts to previously measured standard totals. Non-comparative totals indicate failure(s). They have migrated to the board edge along particular circuit paths. Troubleshooting is performed by backtracking non-comparative counts to their source. Troubleshooting is aided in closed loop failures or in cases where initialization has been prevented through the use of the TRENDAR 200 IC TESTCLIP. Part or all of the FAULTRACK 200 troubleshooting procedure can become a subsidiary technique to the FAULTRACK 1000.

Refer to the flow diagram of Figure 12. The operator checks the count of the first circuit output at (1). If it passes the next is tested. When a non-comparative ("failed") count is detected, we move to (2) and check input counts. If all input counts are normal, we move to (3), perform Node Analysis, repair the board or replace the defective IC and move to the next board output.

If an input has a failed count, the operator backtracks to the preceding IC at (4) and tests its output. If the count is normal, an open circuit or virtual contact on the signal path is indicated. A failed count leads to (5) which, as in (2) has IC inputs checked. If no count failures occur, we move back to (3) and perform Node Analysis on the failed output.

In some situations the operator may backtrack failed inputs and find himself back at an IC he has recently checked. Thus, at (7) he is in a loop and performs a loop test of the IC's using the TRENDAR 200 IC TESTCLIP. This test will have him perform Node Analysis for a detected failure. When the last IC has been tested, he returns at (8) to backtracking a failed input or testing the next board output.

At (6), if a loop fault did not exist the operator keeps backtracking his failed counts. In some cases he may arrive at (9) where the failed count occurs at the very input to the board. This indicates that the input circuit path is defective (or there may be a defective contact at the connector). The procedure is repeated at (1) until all board output counts compare.

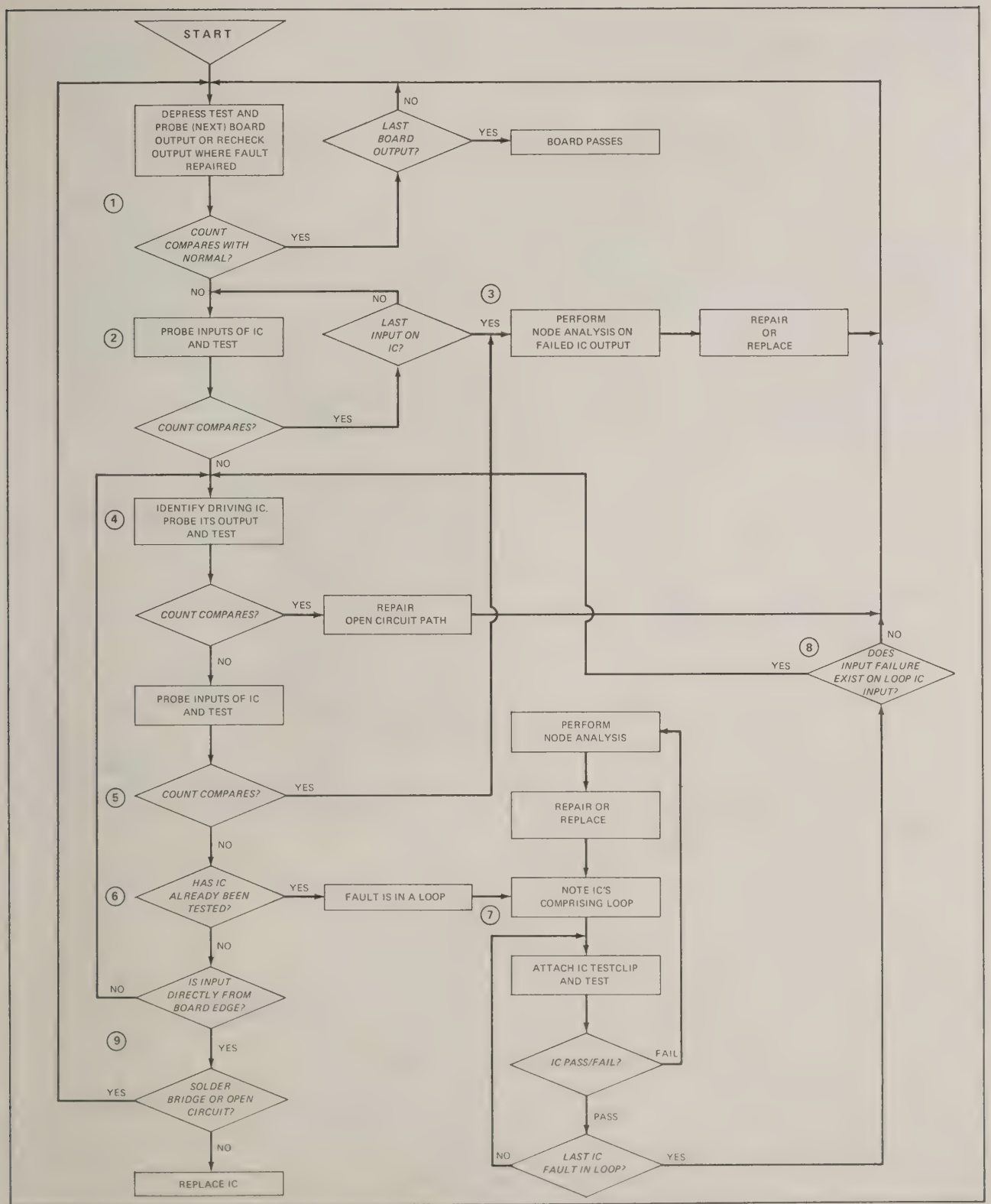

Figure 12. FAULTRACK 1000

FAULTRACK 1000 – EXAMPLE OF TRANSITION COUNTING

Transition counting troubleshooting is based on the fact that a good circuit will exhibit identical repeatable responses to a given input pattern. Identical responses includes logic state responses as tested by the TRENDAR 2000 and TRENDAR 200 or state transition counts ("edges") as measured by the TRENDAR 1000. There is virtually a perfect repetitive correlation between state responses and transition counts. A few obscure fault modes could possibly cause a difference. The transition detection capability of the TRENDAR 1000 uses a form of sampling which ensures highest test validity and confidence.

Consider the circuit of Figure 13. It indicates the correct count totals at each pin. Testing the outputs of IC 1, we measure 1907 counts at pin 16 or board output 36. However, board output 34 measures 72,138 counts as does pin 15. Thus, we have our first non-correspondence . . . too many transitions at this flip-flop latch output. Since the input data came from pin 3, we test again, monitoring the count there. The count is 93,791 instead of 94,148. We suspect a bad node at IC 7 or the fact that an upstream fault is sending incorrect responses to this node. Retesting at pins 4 and 5 of IC 7 we find the correct count at pin 5 and a zero count ("stuck high pin") at pin 4. Testing again at pins 1 and 2 of IC 7, we find a stuck low pin (zero count) at pin 2. Thus, we move upstream to IC 37 pins 4 and 5. Here we find perfect count totals on pin 4 and 5, 1434 and 6 respectively. Pin 6 shows a zero count and is stuck low. At this point, Node Analysis is performed and a solder bridge to ground is discovered. Retesting reveals 1440 counts at pin 6 of IC 37 and the normal 67,721 counts at output 34.

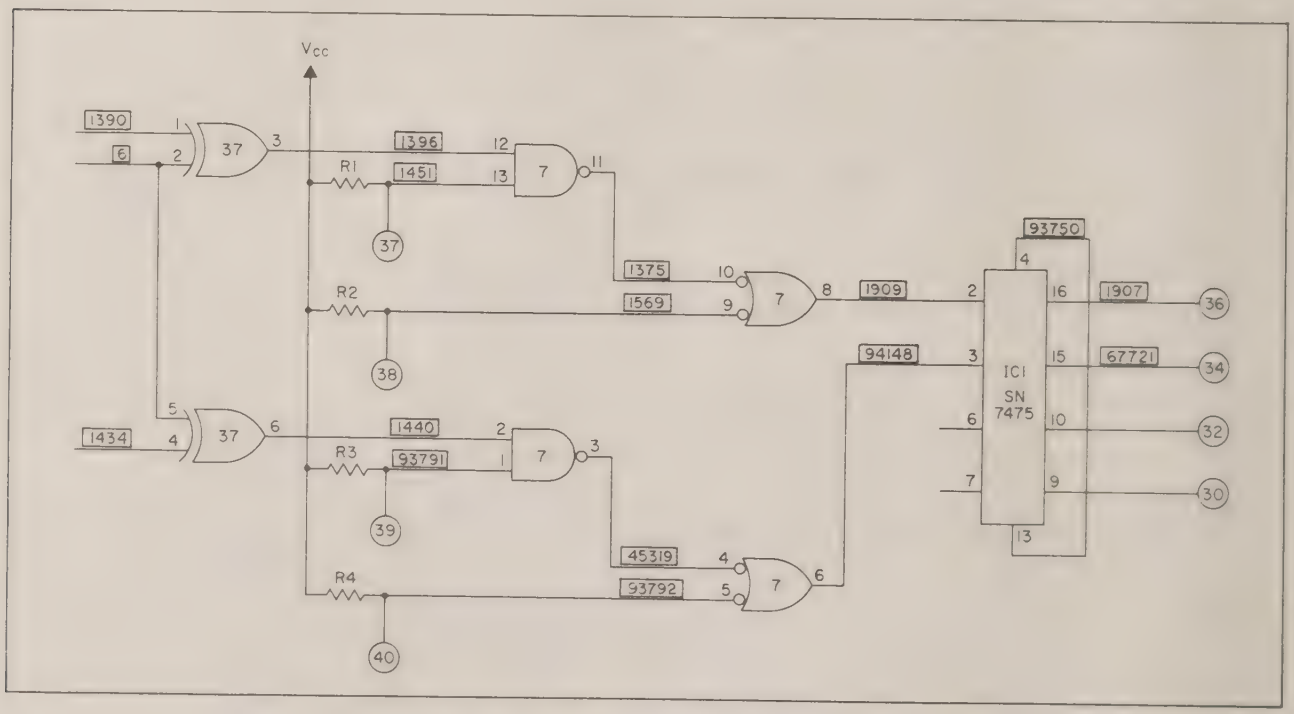

Figure 13. FAULTRACK 1000 EXAMPLE

FAULTRACK 200 - DETAILED DESCRIPTION

If a circuit board is being operated such that its IC's are actively toggling, then a valid functional go-no-go test can be performed using the in-circuit IC test capability of the Fluke TRENDAR 200 IC TESTCLIP. The integrity of the board and the IC's are both verified by performing a functional comparison of IC behavior. If there is a board fault (e.g. solder sliver), it will change the node behavior of the IC driving the slivered path. The TESTCLIP will detect a node failure.

Two systematic approaches can be used. The operator can test all IC's of a type (until all IC types have been tested) or can move from board input IC's toward output IC's. The flow diagram of Figure 14 illustrates the latter method. At (1) the operator starts with an input IC of a given type (e.g. 7408). He checks input toggling behavior at (2) using the Logic Monitor. If an input is not toggling (stuck) and he is at the board edge, he corrects an open circuit between the board input and the IC input. If the operator is checking

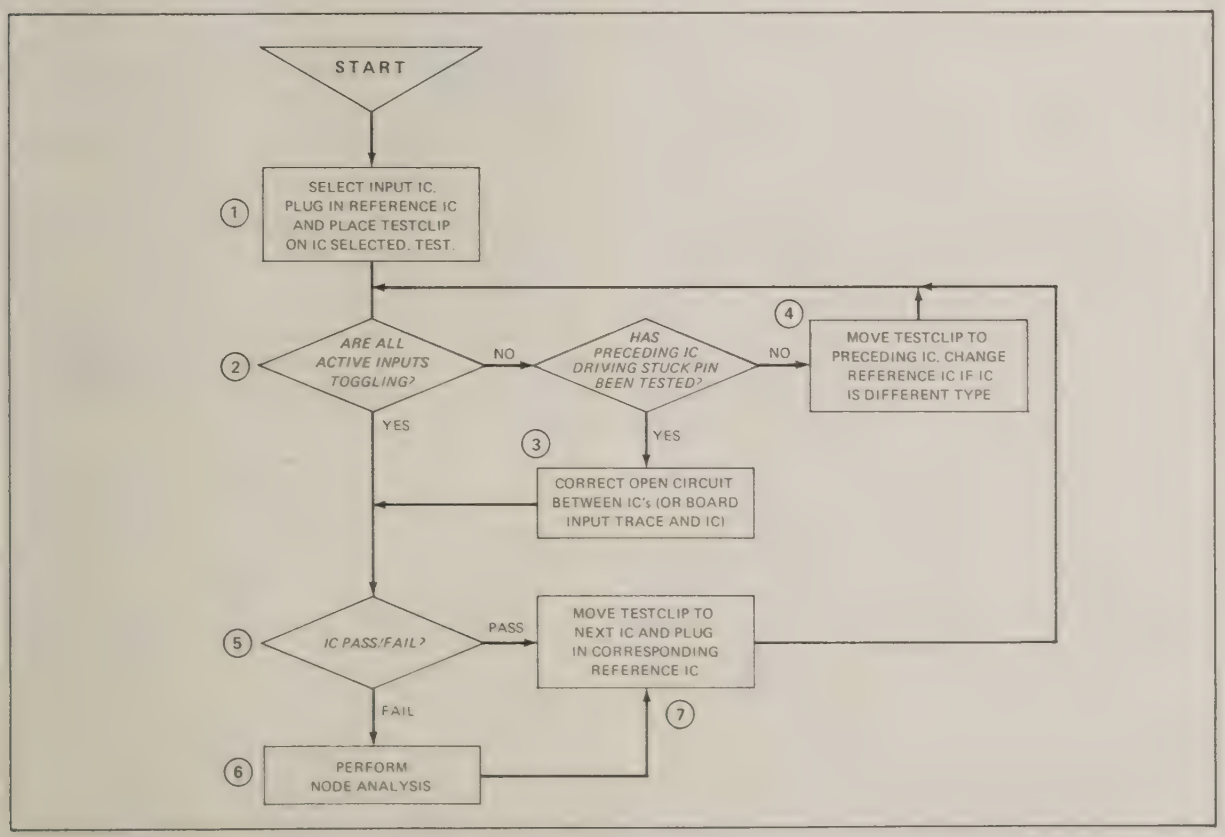

Figure 14. FAULTRACK 200

further in the circuit and finds a stuck input coming from a yet untested IC, he backtracks to that IC and tests it as at (4). When inputs are toggling at (2), a valid functional test can be made at (5). Note, when the TESTCLIP is first connected to a sequential logic element (flip-flop, counter, etc.), momentary failures may occur because the reference IC initially powers up to logic states different from those stored in the UUT. With a good UUT, these first failures will disappear when initialization occurs on both IC's. For example, a reset pulse will initialize counters or clocking of the same data will initialize flip-flops or shift registers. Thus, when a sequential IC fails at (5), the operator must ensure that initialization could have occurred.

If there are no failure indications on the TESTCLIP, the IC passes. Functional failures will cause flashing indications at failing pins. A failure indication is the signal at (6) for Node Analysis.

FAULTRACK 200 — EXAMPLE OF IN-CIRCUIT IC TEST

When a fault sets up a failure which circulates in a loop, in-circuit IC test with the TRENDAR 200 IC TESTCLIP must be used. The simplest and most common case is two gates wired as a storage element (RS flip-flop or latch). A more complex case is presented in Figure 15. Assume the circuit is being tested on a test station. The fault is shown as a trace-to-trace solder bridge and we're assuming that the fault finds its way to the board edge at pin 29 before pin 38 fails. In this case, a failure at pin 29 leads the operator in turn to IC's X,T,W and S. Tracing back from S-11, the operator realizes he is traveling a loop. His procedure will be to move once again through the loop, this time performing an in-circuit IC test on each IC in the loop (T,W, and S). Starting with the TESTCLIP on IC-T, he inserts a reference 7440 into the TESTCLIP and retests. The test will proceed

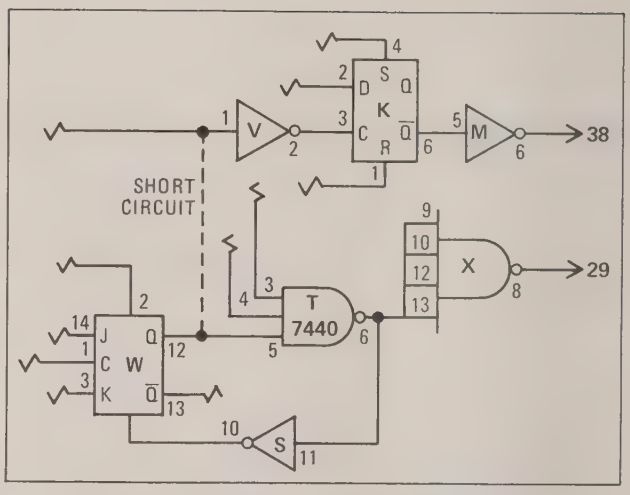

Figure 15. USE OF IN-CIRCUIT IC TEST

through the failure at output number 29 with no failure indicated on the IC Display. This means IC-T is O.K. so he moves the clip to IC-W.

NOTE: If the operator has just done an in-circuit test on an IC with ground and V_{CC} on one pair of pins, e.g. 7 and 14, and then wishes to test another IC type with different power pins, e.g. 4 and 11, the procedure below should be followed to avoid damaging the Reference IC:

1. Disconnect TESTCLIP from IC just tested.
2. Remove the Reference IC just used.
3. Insert the new Reference IC.
4. Clip the TESTCLIP onto the IC to be tested.

The in-circuit IC test of IC-W will show a fault on pin 12. This failure conclusively located the fault node, even though it is circulating in a loop! Node Analysis techniques can now be used to determine the actual defect.

FAULTRACK NODE ANALYSIS

Once a faulty node has been isolated, the actual fault can be traced to one of three causes:

1. A board fault (solder bridge, broken trace or defective solder or feedthrough).
2. A fault in the IC under test (IC whose output node is measured faulty).
3. A fault in a following IC receiving the signals from the faulty output.

Node Analysis is merely a systematic approach to determining the cause, preventing undue "cut and try" effort. The technique is shown in the flow diagram of Figure 16. At (1) we check if the output is toggling. If it is and inputs are active, a failure indication at only an output indicates that the IC is not following its truth table or state diagram. The most likely cause is a short to another active pin or path where the output is fighting another IC's output.

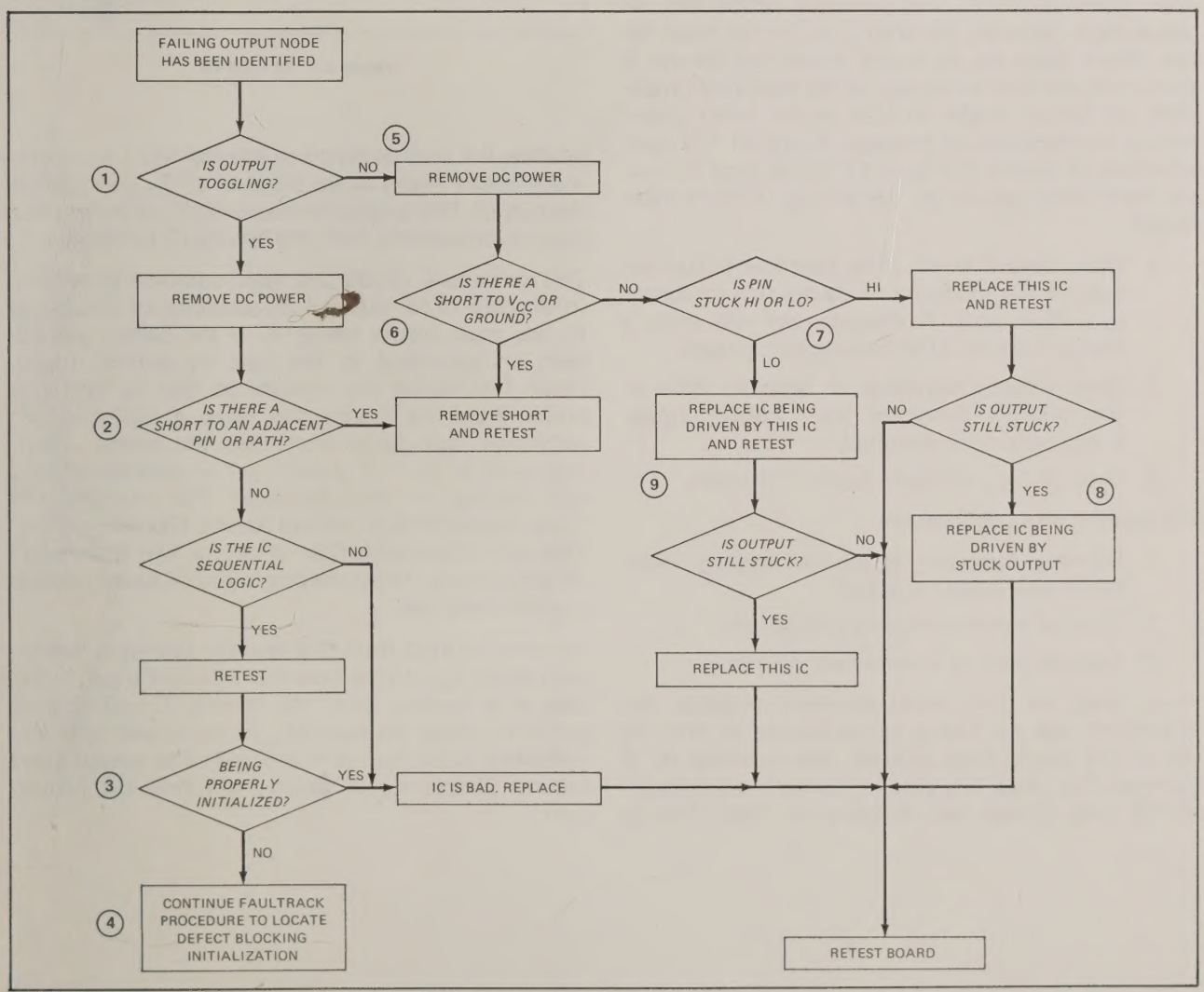

Figure 16. NODE ANALYSIS

This is checked at (2) using a sensitive ohmmeter. At (3) if there are no shorts and proper input activity is present to initialize a sequential IC, we have proof of a defective IC and it is replaced. If at (4) a sequential IC is not receiving proper initialization, the back-tracking of the stuck input activity ensues per the appropriate FAULTRACK procedure.

At (5), we have the case where the faulty node is stuck. We can use a one milliohm or better resolution ohmmeter to zero in on the physical location of a path-to-path short or physical ("hard") short within an IC (6). The ohmmeter will exhibit a minimum or null reading between V_{CC} or ground and the shorted location on the node circuit path. A short to ground will generally not damage an IC. Removal and retest will usually clear the fault. A short to V_{CC} will more often damage the IC and defective action will be noted after removing the short. At (7), we have the case where there are no board shorts and the pin is stuck. Here we take advantage of the statistical probability of failure modes in IC's as the factor determining our replacement strategy. A typical TTL gate schematic is shown in Figure 17. Stuck high failures are most often caused by the driving IC from these causes:

1. Open output bond. (The identical pullup action of the following IC causes this to appear as a high node. A measurement will show a typical 1.5V to 3.0V floating pin voltage).
2. Open steering transistor or defective drive to the steering transistor base, keeping upper totem pole stage saturated.
3. Short to V_{CC} of upper totem pole stage.

The stuck low possibilities are:

1. Steering transistor stuck on keeping lower totem pole stage saturated.
2. Short of totem pole output to ground.
3. Internal short of lower totem pole stage.

Thus, since the first causes are most probable, the procedure calls for changing the driving IC first. At (8), if the stuck node persists, the receiving IC is changed. For stuck low pins we follow the procedure at (9) and change the receiving IC first. This is

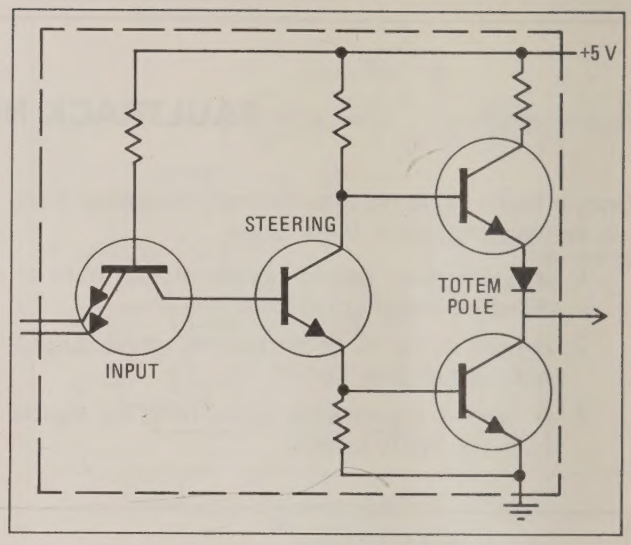

Figure 17. TTL GATE

because the probability of an internal short to ground is somewhat higher at the input of a TTL gate than at the output. If changing the receiving IC does not clear the stuck condition, then the driving IC is changed.

This procedure covers the most common condition. In the case of fan-out and the suspicion of a receiving IC, we must isolate which IC is the cause. This has been accomplished in the past by cutting traces. Fluke TRENDAR has determined that by removing power from the board and using a sensitive high resolution null digital ohmmeter the lowest impedance path to V_{CC} or ground can be determined by a null reading on the ohmmeter. For example, the Fluke Model 8400 DVM will resolve 100 micro-ohms. This will allow resolution of one or two millimeters of circuit trace. Thus, the possibility of board damage is greatly reduced.

We have omitted from this analysis primitive failures such as no V_{CC} to the board or a broken trace. In the case of a broken trace, the driving IC will operate perfectly while the receiving IC input will float and indicate a stuck high as in the case of an output bond failure. Simple signal tracing will find the broken spot.

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